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Study of p-GaN Gate HEMT's Structural and Geometrical Parameters to Realise E-mode HEMT for 750V Switch Operation

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Abstract

E-mode GaN HEMTs are the preferred device configuration for use in high power switching applications and this paper reports a TCAD study on p-GaN gate HEMT structure and device geometry to achieve high breakdown voltage for DC to DC power switching applications. Various HEMT device geometrical parameters have been studied as a function of device electrical parameters i. e. Drain current, threshold voltage Ron and breakdown voltage. The gate -drain spacing of greater than 10 µm is found to be the most critical dimension for achieving high breakdown voltage ~750 V but at the cost of device current handling capability which is found to be decreasing from 960 mA/mm to 900 mA/mm when gate drain spacing of 6um is increased to 10 µm.

Key words: E-mode, GaN, HEMT, Drain current, threshold voltage

I. Introduction

Due to excellent properties of gallium nitride (GaN) and related alloys (e.g., $Al_xGa_{(1-x)}N$) are promising semiconductors for the next generation of high-power and high-frequency devices. AlGaN/GaN based HEMT devices have already established dominance for the applications in MMICs and high-temperature digital ICs, due to the excellent capacity of handling high power and operating at high temperatures and are used in depletion mode device configuration. A higher energy bandgap of semiconductor leads to a higher maxi mum electric field blocking capability. This makes possible the reduction of the device width and therefore its on-resistance and switching times. GaN is the most promising material to achieve the lowest on-resistance and switching times due to its electron saturation velocity, electron mobility, relative permittivity and maximum electric field [1]. Minimum drift region resistance that can be obtained with GaN is about 5.7 times lower than SiC and about 2781 times lower than Si. Thus, GaN material can considerably reduce the conduction losses of the power switching devices. There are still several technological concerns hindering the complete exploitation of these materials. As an example, high electron mobility transistors (HEMTs) based on AlGaN/GaN heterostructures are inherently normally-on (a current will flow between the source and drain even at zero bias to the gate (Vg = 0)) devices. However, normally-off (V_{th}>0) switching devices are preferred in power electronics, due to their inherent safety as they offer more failsafe operation conditions and gate driver circuitry simplicity operation. There are several methods for fabrication of normally off (enhancement mode) device, like recessed gate, fluorine gate HEMT (consisting in the introduction of negatively charged fluorine ions below the gate electrode, either by plasma or ion-implantation processes) cascode configuration [2-4], Mainly p-GaN gate configuration is preferred for reliable switch operation due to its minimum threshold voltage invariability leading to reliable high power switching operation [5-10]. The present paper investigates the detailed simulation studies for the p-GaN gate HEMT device electrical characteristics to arrive at the optimum HEMT structure with suitable material parameters. The effect of device geometrical parameters on drain current, Ron and breakdown voltage is also studied to design a p-GaN gate HEMT suitable for power switching applications up to 750V.

II. HEMT structure and device layout

TCAD Simulation studies are performed to study the E-mode HEMT device characteristics using ATLAS device simulator [11]. The effect of HEMT device geometrical parameters like gate to drain spacing (Lgd), gate to source spacing (Lsd), gate length (Lg) and gate width (Wg) on device electrical characteristics has been investigated systematically. A basic device layout is finalised as shown in fig.1 to investigate the electrical performance. p-GaN gate HEMT off state characteristics and output characteristics are simulated and analysed. Details about the structure and the simulated characteristics are presented in the following section.

The typical HEMT layer structure of p-GaN/AlGaN/GaN device is shown in fig.2 (where p-GaN : Mg as the p type impurity). To achieve an efficient depletion of the 2DEG and Vth > 0, the properties of

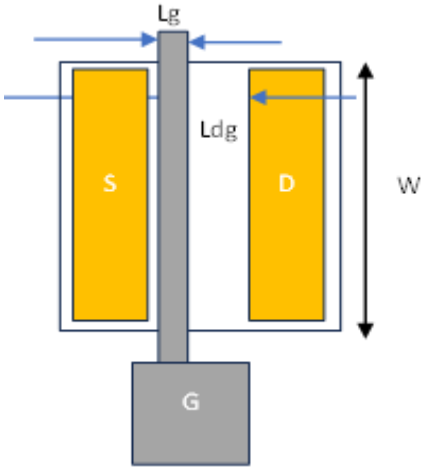

Fig.1. Basic device layout used for the study

normally-off p-GaN/AlGaN/GaN heterostructure the AlGaN barrier layer thickness is in the range of 10–18 nm, while the Al concentration is in the order of 18-22% and high doping level of the p-GaN layer (> 10^{18} cm^{-3}) is also required for an efficient depletion of the region at the metal-gate/p-GaN interface. A typical e-mode hetero-structure with top p-GaN layer of 80-90nm thickness was chosen to completely deplete the channel under the p-GaN gate at zero gate voltage.

- p-GaN:Mg, Mg~3E^{19}/cm^3,
- Cap1 layer: 90nm
- GaN undoped cap2 layer: 5nm
- $Al_xGa_{(1-x)}N$ barrier: x=22% ; 18nm
- Undoped GaN channel: 500nm
- GaN buffer :3.0µm
- AlN nucleation layer: 40 nm
- SiC substrate

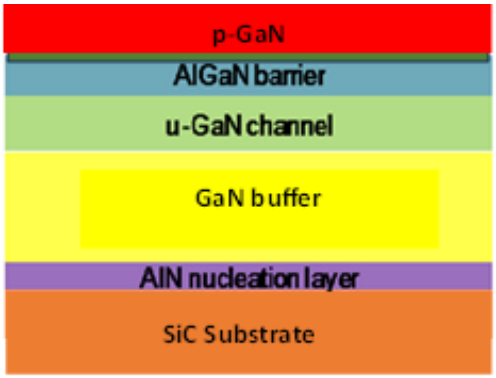

Fig.2. E-mode HEMT structure details

Table I. Device parameters used for the study

S. No	Parameter	Value (µm)
1.	Gate length, Lg	2
2.	Gate source spacing, Lsg	2
3.	Gate drain spacing, Lgd	4, 6, 10, 12
4.	p-GaN length, Lp	4
5.	Gate width, Wg	100
6.	p-doping	$3x10^{19}cm^{-3}$

TCAD simulation studies were carried out by selecting a basic device layout and authenticated by using ATLAS device simulator. The simulation deck was calibrated using published experimental result in IEEE EDL-42, pp-22, Jan 2021[12}. The device parameters used for simulation are given in table I. The device geometrical parameters are selected based on the presently existing fabrication capability inhouse.

III. Results and Discussion

In the lateral device like GaN HEMT, in addition to material parameters like 2DEG density (Ns), carrier mobility (µ) and sheet resistance (Rs), the device geometrical parameters i.e. gate to drain spacing (Lgd), gate to source spacing (Lsd), gate length (Lg) and gate width (Wg) are very critical for achieving desired device DC characteristics. The effect of these

geometrical parameters has been studied in detail on device electrical characteristics and results are presented below.

A. Transfer Characteristics at Vds = 10 V: The drain current (Ids) is showing direct dependency on Lgd and decreasing with its increase mainly due to increase in source drain resistance. The maximum value of current obtained is ~ 0.96 A/mm at Lgd=4 µm and is clearly shown in fig. 3.

- Red - Lgd: 4 µm (Id-Max: 0.96 A/mm)
- Green - Lgd: 6 µm (Id-Max: 0.94 A/mm)
- Blue - Lgd: 10 µm (Id-Max: 0.92 A/mm)
- Sky Blue - Lgd: 12 µm (Id-Max: 0.90 A/mm)

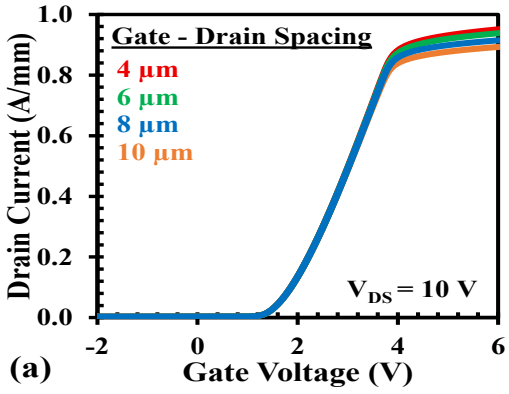

Fig.3. Drain current (Ids) as a function of gate drain spacing (Lgd)

B. **Output Characteristics:** Fig.4 shows the simulated device output characteristics as function of Lgd which clearly indicates increase in Ron with increase in Lgd.

- Red - Lgd: 4 µm
- Green - Lgd: 6 µm
- Blue - Lgd: 8 µm
- Sky Blue - Lgd: 10 µm

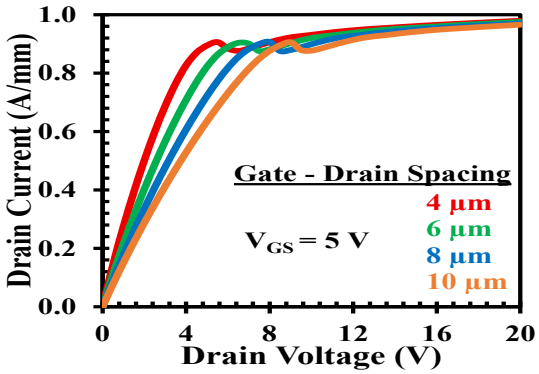

Fig.4. Simulated device output characteristics

C. **Output Characteristics for Lgd: 4µm as a function of gate source voltage:**

Fig.5 shows the variation of output characteristics as a function of gate source voltage. The graph clearly indicates that the saturated Ids current is increasing with gate voltage due to increase in channel opening as result of reduction in depletion region under gate.

- Blue: Vgs + 5 V
- Green: Vgs + 3 V
- Red: Vgs + 1 V

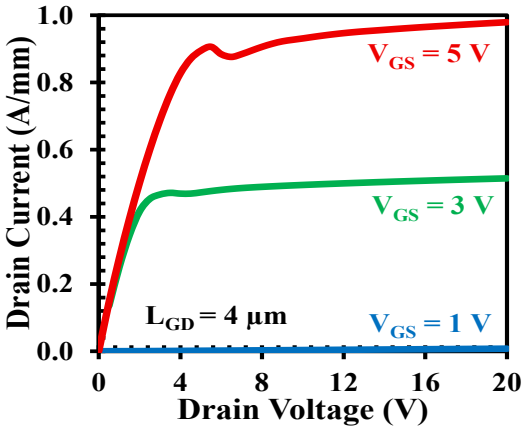

Fig.5. Variation of output characteristics as a function of gate source voltage (Vgs).

D. **Impact of gate drain spacing (Ldg) on Breakdown voltage:** Fig. 6 depicts effect on Lgd on Vboff that represents breakdown voltage in device off-state condition, and is one of the very critical parameter for power switching application**.** It clearly shows the strong dependency of breakdown voltage on Lgd and increases with increase in Lgd. The

desired breakdown of > 750V is achieved for the Lgd ~10 µm.

- Red - Lgd: 4µm (Breakdown: 480 V)
- Green - Lgd: 6µm (Breakdown: 630 V)
- Blue - Lgd: 8µm (Breakdown: 710 V)
- Sky Blue - Lgd: 10µm (Breakdown: 750 V)

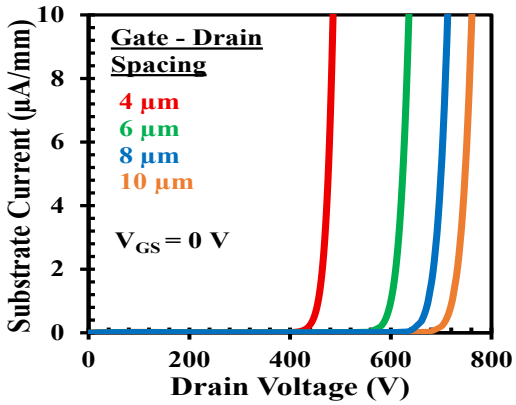

Fig. 6. Device breakdown voltage as a function of Lgd

The simulated results are consistent and well within the desired range. For a lateral device like HEMT, Lgd is very critical parameter for breakdown voltage and has been varied from 4-10µm in current study to arrive at the optimum value of breakdown voltage ≥ 750V targeting EV application. This range of Lgd was selected to have minimum impact on device on-state device characteristics. Breakdown voltage is increasing with Lgd and reaches to a value ~ 750V for gate drain spacings of greater than equal to 10µm. It is also worth mentioning that HEMT material parameters are equally important for achieving high breakdown voltage with good on-state device characteristics. Therefore, the thickness and Al concentration of AlGaN barrier layer is chosen carefully to meet the requirement of reasonable 2DEG density ≥ 8e12 cm^{-2} and mobility ~1800 cm^2/V. sec.

Conclusions

A p-GaN gate HEMT device basic layout/structure has been optimised using TCAD simulation. Several HEMT device geometrical parameters have been studied and a basic device layout has been finalized. The device electrical parameters are strong function of HEMT material and device geometrical parameters. It is also evident from the simulated results that the most critical parameter for power switch i.e. breakdown voltage is greatly influenced by gate to drain spacing in a lateral device like GaN HEMT. The Lgd spacing of greater than 10um is an essential requirement in E-mode HEMT for achieving high breakdown voltage ~750V but at the cost of device on state performance that gets affected in terms of increased Ron. Therefore, it is essential to minimize Lgd in the device layout while maintaining the desired breakdown.

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