Performance of the AlGaN/GaN HEMT with Sunken Source Connected Field Plate under High Voltage Reverse Bias Step Stress

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Abstract: The manuscript investigates the DC performance of conventional HEMT and Sunken Source Connected Field Plate (SSC-FP) HEMT reliability under reverse bias step stress. To assess the electrical performance of the device at the gate terminal is subjected to a high reverse bias step stress up to – 40 V with an increase of – 5 V step. A higher degree of ON–state resistance (R_{ON}) degradation is observed in the conventional HEMT than in the SSC-FP HEMT device. Post-stress drain to source current (I_{ds}) degradation is ~11% and ~6% in non-FP and with SSC-FP devices respectively. In conventional devices when gate voltage (V_{GS}) is up to -20V, the device leakage current is recoverable but after that, the gate current increases exponentially and becomes noisy. In SSC-FP devices, this behavior is shown after gate voltage -30V.

Keywords: AlGaN/GaN HEMT, Threshold Voltage Shift, OFF–State Stress, Reliability.

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Introduction: The birth of AlGaN/GaN High Electron Mobility Transistors (HEMTs) represent a significant breakthrough in the field of semiconductor technology, particularly for applications requiring high power, high frequency, and high-temperature operation [1-4]. These devices exploit the unique properties of Gallium Nitride (GaN), a wide-bandgap semiconductor, and the AlGaN/GaN heterojunction to achieve superior performance compared to traditional silicon-based transistors [5, 6]. GaN's wide bandgap of 3.4 eV allows for higher breakdown voltages, greater power density, and improved thermal stability, making it an ideal choice for demanding environments such as radar systems, satellite communications, and power electronics [7, 8]. New applications in 5G communication infrastructure, electric vehicles, and renewable energy systems are emerging as key areas where these devices could drive transformative technological advancements [9-12]. Moreover, the integration of AlGaN/GaN HEMTs with other semiconductor technologies, such as silicon carbide (SiC) and diamond, holds promise for further enhancing the power handling capacity and efficiency of these devices [10].

The structure of AlGaN/GaN HEMTs is particularly noteworthy for its ability to generate a high-density two-dimensional electron gas (2DEG) at the heterojunction interface [11]. This 2DEG, formed without doping, enables extremely high electron mobility, leading to low on-resistance and fast switching speeds. As a result, AlGaN/GaN HEMTs have rapidly gained traction in the defense, telecommunications, and automotive industries, where performance and efficiency are paramount [12-14].

Looking toward the future, ongoing research into AlGaN/GaN HEMT devices is expected to unlock even more advanced capabilities. Efforts are focused on improving device reliability, thermal management, and scalability for mass production. However, improving their reliability under high operating voltage conditions remain a critical challenge. The introduction of a Sunken

Source Connected Field Plate (SSC-FP) in AlGaN/GaN HEMTs has proven to be an effective solution that enhances device performance and reliability [13, 14]. This design has a metal plate parallel to the gate terminal and is connected to the source through the mesa region, significantly reduces the parasitic capacitances (C_{gs} and C_{gd}) compared to other field plate technology. SSC-FP suppresses electric field peaks at the gate edge towards the drain terminal, and improves the breakdown voltage, which is crucial for high-power applications such as X-band radar systems and power amplifiers in satellite communications [10-12]. The future research will likely focus on further optimizing this structure for better thermal management and scalability, ensuring that AlGaN/GaN HEMTs remain a keystone of high-power electronics.

A study by Bothe *et al.,* demonstrated that HEMTs with an SSC-FP exhibit over 10 W/mm saturated output power and superior reliability, with an estimated lifetime exceeding 6×10^7 hours at 225°C, a more than two-fold increase over conventional designs [14]. Also, Zhu *et al*. reported that FP helps mitigate the detrimental effects of the inverse piezoelectric effect and trapping phenomena, which are often exacerbated under reverse-bias stress conditions [15]. This work investigates the performance of non-FP and SSC-FP HEMT devices under high reverse bias step stress.

The article is structured as follows: Section 2 presents the details of the device structure and fabrication process. Section 3 compiles the DC IV measurements and reliability studies and summarizes them with extracted parameters. Finally, the manuscript concluded in Section 4.

2. Experimental Methodology: AlGaN/GaN HEMTs were grown on SiC substrates using metal-organic chemical vapor deposition technique, with 25nm thick $Al_{0.25}Ga_{0.75}N$ on a 2µm semi-insulating GaN buffer. Standard Ti/Al/Ni/Au source/drain ohmic contact metallization is done using the e-beam evaporation technique and annealed at 820 ˚C for 30 sec. Device isolation is carried out using the nitrogen implantation process. T-shaped Ni/Au gate contact were fabricated using slit etching. Devices were passivated using 100nm SiN_x deposited by plasma-enhanced CVD [13]. HEMTs with gate length, source-drain spacing, gate-drain spacing, and gate width of 0.4, 6, 4.6, and 100 µm, respectively. Schematic of the non-FP and with SSC-FP is shown in Fig.1 (a & b). The process flow of the fabrication of the devices is shown in Fig. 2. The measurement procedure is shown in Fig. 3, the fabricated devices were subjected to OFF state step stress at room temperature. Electrical measurements were carried out using Semiconductor Parametric Analyzer SCS-4200A.

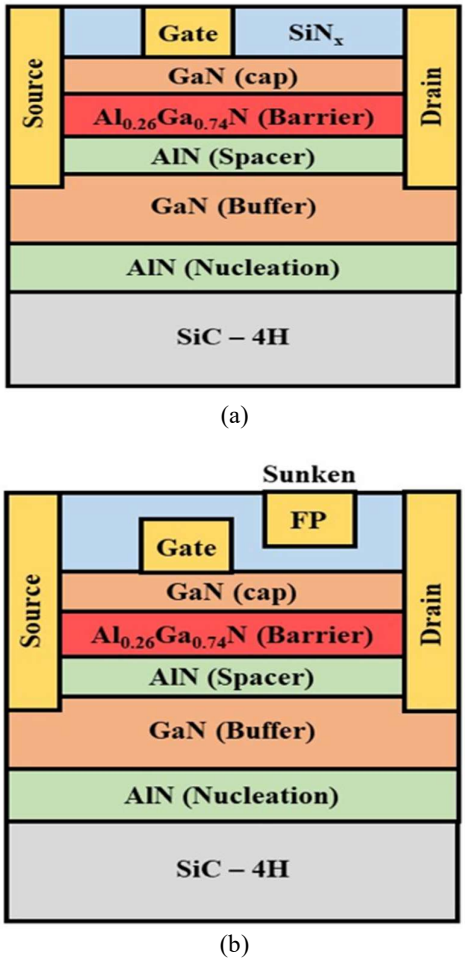


Figure 1. (a) and, (b) Schematic representations of the conventional (non-FP) and the SSC-FP HEMT device, respectively.

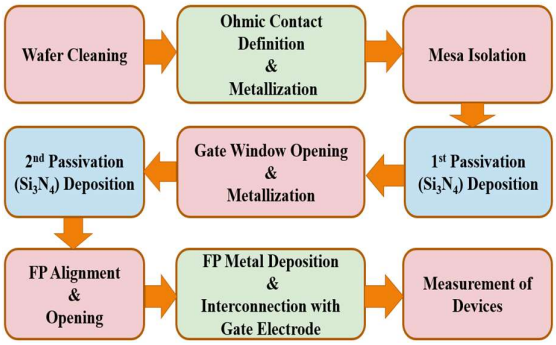


Figure 2. Flow chart of the fabrication of AlGaN/GaN HEMT devices.

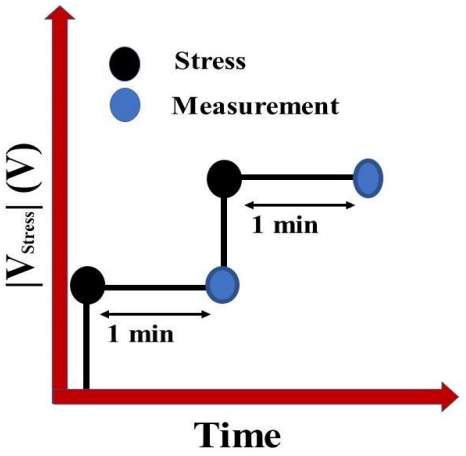


Figure 3. Shows the measurement procedure of the device.

As shown in Fig. 3, device pre-measurement is carried out and then the gate reverse bias is increased with the step of -5V. Devices were subjected to 60 second stress cycles, and electrical measurements were taken after each stage.

3. Results & Discussions:

3.1 Two Terminal Schottky Diode measurements: Forward and reverse Characteristics of the Schottky is carried out, as shown in Fig. 4 (a & b). The Φ_B and η are calculated using the thermionic emission (TE) model by using the standard diode equations (1) and (2):

$$I = I_S \left[\exp\left(\frac{qV - IRD}{\eta kT}\right) - 1\right] \quad (1)$$

$$I_S = AA^*T^2 \exp\left(-q\,\Phi_B / kT\right) \quad (2)$$

where,

q= carrier charge,

k= Boltzmann's constant,

T= Temperature,

Φ_B= Schottky barrier height

η = Ideality factor,

A= Diode area,

I_S= Reverse saturation current

IR_D = Voltage drop across the diode, and

A*= Richardson constant for AlGaN.

Table 1 summarizes the extracted parameters before and after stress.

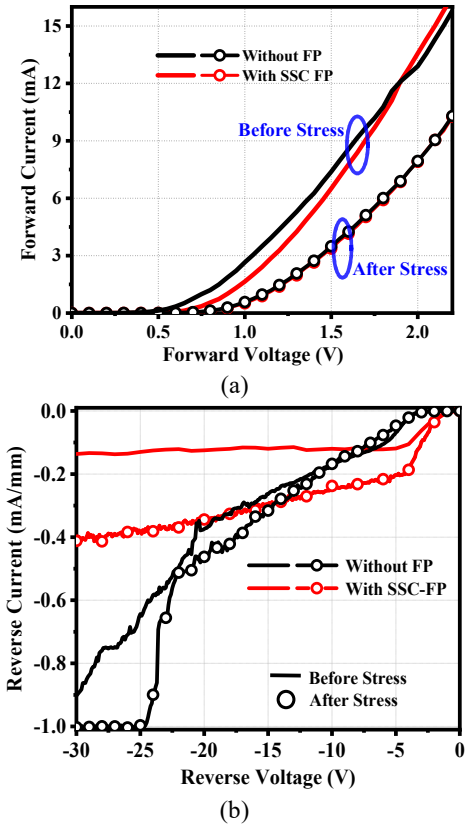


Figure 4. Comparison of (a) Forward, and (b) Reverse two terminal Gate characteristics of Non-FP and SSC-FP HEMT devices after step stress (V_g=-40V).

Table 1 Comparison of two terminal (Schottky Parameters) of the Non-FP and SSC-FP HEMT devices.

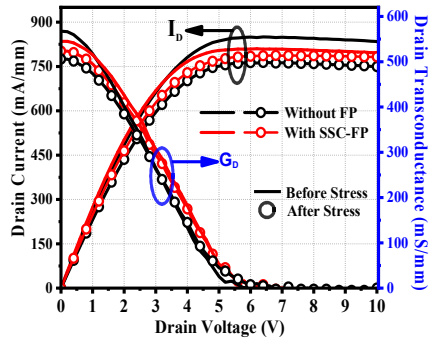
Device	Diode Parameters			
	Before stress		After stress	
	Φ_B (eV)	η	Φ_B (eV)	η
Without FP	0.910	1.15	0.856	1.56
With SSC-FP	0.905	1.16	0.867	1.47

As Fig. 4 shows the degradation in the Schottky parameters after step stress. The continuous stress at the gate (Ni/Au) leads to Nickel diffusion and corresponds to the degradation of the gate edge [17].

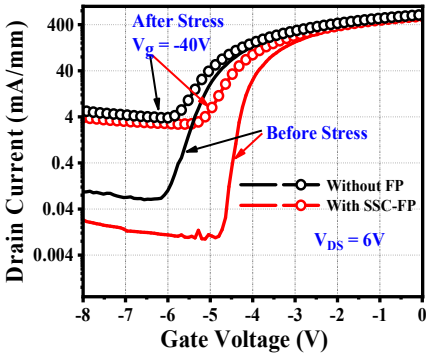
3.2 Three Terminal Device Measurements:

- **Reverse Bias Step Stress at the Gate Terminal:** In the step stress measurement technique, stress is applied incrementally overtime at the gate terminal. In this experiment, the V_{GS} was stepped by -5V. The device's leakage current was measured for 60 seconds at each step stress. The results of high reverse bias gate voltage step stress are shown in Fig. 5. The findings suggest that leakage remains recoverable up to a gate voltage of -20V and -30V, in conventional and SSC-FP devices respectively, which attributed to the trapping of electrons beneath the gate region. In non-FP devices at V_{gs} =-20V, the gate current becomes noisy and undergoes a significant increase, signaling the degradation in device performance while in the SSC-FP device, it is observed after V_{gs}=-30V.

As high voltage is applied to the gate terminal, the vertical electric field in the device increases which induces leakage paths in silicon nitride and AlGaN barrier which causes a rise in the gate current [17, 18]. Also, it is described that a high electric field deteriorates the original lattice parameters of the barrier layer and induces an inverse piezoelectric phenomenon [16]. Also, Zanoni *et al.* [18] reported through electroluminescence (EL) studies that hot-spot formation at the gate edge under high reverse bias contributes to the rise in leakage current. DC characterization is carried out before and after each step of stress to observe the current collapse phenomenon, which manifests in the form of an increase in the dynamic resistance (R_{ON}) of the device. Fig. 5 (a & b) shows the increase in the R_{ON}, V_{TH} shift, and increase in off-state leakage current post-stress in both non-FP and FP devices. Post stress a reduction in drain transconductance (g_D) and gate transconductance (g_M) is also observed as shown in Fig. 5 (a) and Fig. 5 (c) respectively. Degradation in gate contact and defects generation can be observed with the increase in gate leakage current which is shown in Fig. 5(d) with time. Table 2, explains the change in the parameters post-step stress.



(a)



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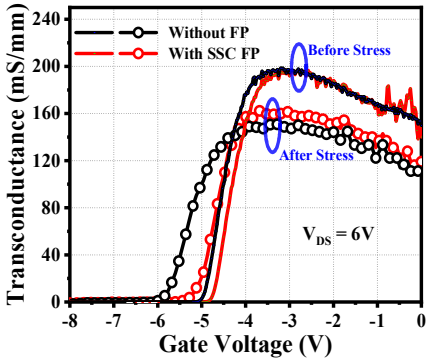
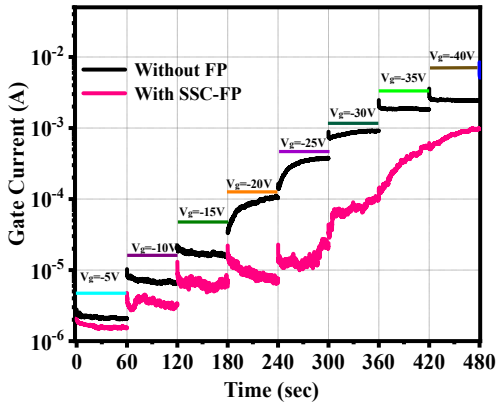


(c)



(d)

Figure 5. Post reverse bias step stress scheme, (a) Output characteristics, (b) & (c) shows transfer characteristics, and (d) gate current as a function of transient time.

Table 2 summarizes the change in device parameters before and post-stress.

Parameters		Device	
		Without FP	With SSC-FP
I_{DS} (mA/mm)	Before Stress	850	830
	After Stress	760	778
	Δ (%)	10.6	6.3
R_{ON} (Ω·mm)	Before Stress	4.56	4.55
	After Stress	6.25	5.02
	Δ (%)	37.0	10.3
V_{TH} (V)	Before Stress	-4.98	-4.85
	After Stress	-5.82	-5.25
	Δ (%)	16.8	8.24
G_m	Before Stress	190	190
	After Stress	148	160
	Δ (%)	22.1	15.8

Here, delta (Δ) represents the change in the parameters. A remarkable degradation is observed in the conventional HEMT as compared to the SSC-FP HEMT devices.

4. Conclusions: A comparative study of conventional HEMT and SSC-FP HEMT devices is studied. Post reverse bias step stress, the electrical performance of the device is investigated. Conventional devices are more vulnerable to degradation under high electric fields compared to SSC-FP HEMT devices. The SSC-FP device reduces the peak of the vertical electric field which prevents the degradation of the device parameters like threshold voltage (V_{TH}) shift and R_{ON}. Post reverse bias step stress up to -40V, the degradation of ~11% and 37% in I_{DS} and R_{ON}, respectively in the case of the conventional device against the ~6% and ~10% degradation recorded in the SSC-FP HEMT device the I_{DS} and R_{ON}, respectively. The SSC-FP design introduces several reliability benefits under high reverse-bias step stress. The reduction in the electric field intensity near the gate edge leads to a lower likelihood of premature device failure, which is particularly critical when operating at high drain-source voltages.

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CRedit Author Statement

Chanchal: Conceptualization, Methodology, Visualization, Data analysis and interpretation, Investigation and Writing – Original Draft.

Amit Malik: Visualization, Reviewing and Editing Supervision, Technical Inputs.

Robert Laishram: Technical Inputs and Proofreading.

Dipendra Singh Rawal: Supervision, Writing- Reviewing and Editing, Validation, Technical Inputs and Resources.

Manoj Saxena: Supervision, Proofreading, Writing- Reviewing and Editing, Technical Inputs.

Conflict of Interest: Authors declare No conflicts of interest.

5. References:

[1] S. Krause *et al*., AlScN/GaN HEMTs Grown by Metal-Organic Chemical Vapor Deposition With 8.4 W/mm Output Power and 48 % Power-Added Efficiency at 30 GHz, IEEE Electron Device Letters, vol. 44, no. 1, pp. 17-20, Jan. 2023. DOI: 10.1109/LED.2022.3220877.

[2] N. Collaert *et al.*, III-V/III-N technologies for next generation high - capacity wireless communication, International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2022, pp. 11.5.1-11.5.4. DOI: 10.1109/IEDM45625.2022. 10019555.

[3] P. Wang *et al.*, Evaluation of Power and Linearity at 30 GHz in AlGaN/GaN HEMT Fabricated by Integrating Transistors with Multiple Threshold Voltages, IEEE Transactions on Electron Devices, vol. 71, no. 3, pp. 1421-1427, March 2024. DOI: 10.1109/TED.2023.3347710.

[4] A. Hickman *et al.*, 2.2 W/mm at 94 GHz in AlN/GaN/AlN High Electron Mobility Transistors on SiC, Physica Status Solidi A, vol. 220, no. 16, January 2023. DOI: 10.1002/pssa.202200774.

[5] A. S. Razeen *et al*., Structural, optical, and electrical characterization and performance comparison of AlGaN/GaN HEMT structures with different buffer layers, Vacuum, Vol. 219, art. no. 112704, January 2024. DOI: 10.1016/j.vacuum.2023.112704.

[6] D. Y. Chen *et al.*, Impact of the Channel Thickness on Electron Confinement in MOCVD-Grown High Breakdown Buffer-Free AlGaN/GaN Heterostructure, Physica Status Solidi A, Vol. 220, no. 16, art. no. 2200496, September 2022. DOI: 10.1002/pssa.202200496.

[7] N Islam *et al*., Reliability, Applications and Challenges of GaN HEMT Technology for Modern Power Devices: A Review, Crystals, Vol. 12, Issue 11, 2022. DOI: 10.3390/cryst12111581.

[8] A. K. Visvkarma *et al.*, Comparative study of Au and Ni/Au gated AlGaN/GaN high electron mobility transistors, AIP Advances, vol. 9, no. 12, art. no. 12531, December 2019. DOI: 10.1063/1.5116356.

[9] D. M. Fleetwood, X. Li, E. X. Zhang, R. D. Schrimpf and S. T. Pantelides, Low-Frequency Noise Due to Iron Impurity Centers in GaN-Based HEMTs, IEEE Transactions on Electron Devices, vol. 71, no. 2, pp. 1024-1030, Feb. 2024, doi: 10.1109/TED.2023.3347212.

[10] Nicholas C. Miller *et al.,* A Survey of GaN HEMT Technologies for Millimeter-Wave Low Noise Applications, Vol. 3, IEEE Journal of Microwaves, 2023. DOI: 10.1109/JMW.2023.3313111.

[11] X. Ding *et al.*, Gate leakage mechanisms of the AlGaN/GaN HEMT with fluorinated graphene passivation, Materials Science in Semiconductor Processing, vol. 162, art. no. 107502, August 2023. DOI: 10.1016/j.mssp.2023. 107502.

[12] Wei-Min Wu *et al*., ESD Failures of GaN-on-Si D-Mode AlGaN/GaN MIS-HEMT and HEMT Devices for 5G Telecommunications, 2021 43rd Annual EOS/ESD Symposium (EOS/ESD), Tucson, AZ, USA, 2021, pp. 1-7. DOI: 10.23919/EOS/ESD52038.2021.9574716.

[13] Chanchal *et al*., Physical insights into the reliability of sunken source connected field plate GaN HEMTs for mm-wave applications, Volume 148, 115170, Microelectronics Reliability (2023). DOI: 10.1016/j.microrel.2023.115170.

[14] K. Bothe *et al.,* Improved X-Band Performance and Reliability of a GaN HEMT with Sunken Source Connected Field Plate

Design, IEEE Electron Device Letters, March 2022. DOI: 10.1109/led.2022.3146194.

[15] Q. Zhu *et al.,* Investigation of Inverse Piezoelectric Effect and Trap Effect in AlGaN/GaN HEMTs under Reverse-Bias Step Stress at Cryogenic Temperature, IEEE Access (2020). DOI: 10.1109/ACCESS.2020.2975118.

[16] K Mazumdar *et al.,* Nanocrack formation due to inverse piezoelectric effect in AlGaN/GaN HEMT, Superlattices and Microstructures, Vol. 125, Pages 120-124,2019.DOI: 10.1016/j.spmi.2018.04.038.

[17] J. A. del Alamo, and Jungwoo Joh., GaN HEMT reliability. Microelectronics reliability 49, no. 9-11 (2009): 1200-1206. https://doi.org/10.1016/j.microrel.2009.07.003.

[18] Enrico Zonani *et al.,* Localized damage in AlGaN/GaN HEMTs induced by reverse-bias testing. IEEE Electron Device Letters 30, no. 5 (2009): 427-429. https://doi.org/10.1109/LED.2009.2016440.